

## Nickel Barrier Termination Type

### △ Features

- Small in size and wide capacitance range.
- Superior humidity characteristic and long life thanks to the monolithic construction.
- Three layer terminals are made of metal, excellent solderability and high resistance to migration.
- Low inductance and excellent frequency characteristics enable a circuit with parameters nearly to the designed theoretical values.

### △ Part Numbering

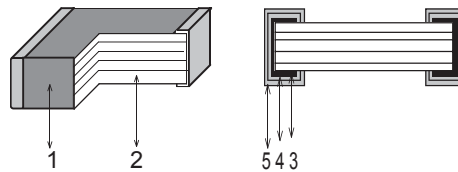
**CMC 0805 CG 102 J 1H**  
 (1) (2) (3) (4) (5) (6)

- (1) Type
- (2) EIA size code
- (3) Temperature characteristics
- (4) Nominal capacitance
- (5) Capacitance tolerance
- (6) Rated voltage

### △ Applications

- General electronic equipment.
- Class I (T.C. Type) Temperature compensation.
- Class I (T.C. Type) Tuned Circuits and Filters.
- Class II (Hi-K type) By pass and coupling.

### △ Construction



NO.	Name	Material
1.	Ceramic Dielectric	Ceramics
2.	Inner Electrode	Palladium
3.	Substrate Electrode	Silver
4.	Intermediate Electrode	Nickel
5.	External Electrode	Solder

### (3) Temperature characteristics

#### Class I (Temperature compensating type)

Code	C0G(CG)
Temp. range	-55 to 125°C
Temp. Coeff.	0 ± 30ppm/°C

#### Class II (High dielectric constant type)

Code	X7R(XR)	Z5U(ZU)	Y5V(YV)
Temp. range	-55 to 125°C	+10 to 85°C	-30 to 85°C
Cap. change	±15%	+22 to -56%	+22 to -82%

### (4) Nominal Capacitance Designation

Stated in three digits and in units of pico farads (pF). The capacitance shall be expressed in a 3 digits code. The first and second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier. However, when capacitance is below 10pF there are decimal digits included, they are stated as D. Please check examples below:

Symbol	Capacitance (pF)
D50	0.5
D75	0.75
1D5	1.5
100	10
101	100

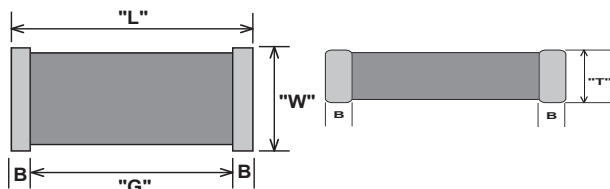
### (5) Capacitance Tolerance

J = ±5% K = ±10%

### (6) Rated Voltage

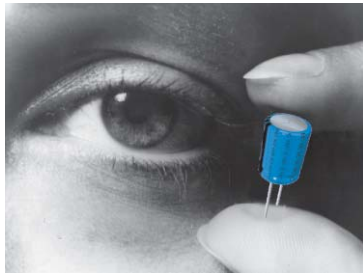
1H = 50V

### (2) Size and Dimensions



Size	Dimensions in (mm) [Brackets indicate in inches]				
	L	W	T max.	B min.	G min.
<b>0402</b>	1±0.05 [0.39±.002]	0.5±0.05 [0.20±.002]	0.5 [0.20]	0.15 [.006]	0.3 [0.12]
<b>0603</b>	1.6±0.1 [.063±.004]	0.8±0.1 [.031±.004]	0.9 [.035]	0.2 [.008]	0.3 [.012]
<b>0805</b>	2.0±0.2 [.079±.008]	1.25±0.2 [.049±.008]	1.45 [.057]	0.2 [.008]	0.5 [.020]
<b>1206</b>	3.2±0.2 [.126±.008]	1.6±0.2 [.063±.008]	1.30 [.051]	0.2 [.008]	1.0 [.039]
<b>1210</b>	3.2±0.4 [.126±.016]	2.5±0.3 [.098±.012]	1.90 [.075]	0.3 [.012]	1.0 [.039]
<b>1812</b>	4.5±0.5 [.177±0.20]	3.2±0.4 [.126±.016]	1.90 [.075]	0.4 [.016]	2.0 [.079]
<b>2220</b>	5.6±0.5 [.220±.020]	5.0±0.5 [.197±.020]	1.90 [.075]	0.4 [.016]	2.0 [.079]

Surface Mount Capacitors



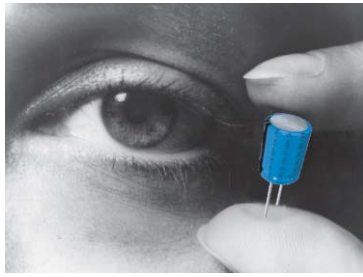
Multilayer Ceramic Chip Capacitors  
Performance Specifications

1. Electrical

Dielectric Code	DIA IEC	COG 1BCG	X7R 2R1		
Temperature Characteristics	*1	0±30ppm/°C, C>20pF +120 ~ -40ppm/°C, C 20pF	ΔC±15% maximum over -55°C to +125°C		
Operating Temperature Range		-55°C to +125°C	-55°C to +125°C		
Measuring Conditions for Capacitance and D.F.	*2	1 MHz, 1 Crms, C 1000pF 1 MHz, 1 Crms, C > 1000pF	1KHz, 1 Vrms		
Dissipation Factor (D.F.) and Tangent of Loss Angle (tan δ)		0.1% for C 30 pF 100%/(400+20C) for C < 30pF	rated voltage		
			2.5%		50V
			3.5%	25V	16V
			5.0%	10V	6.3V
Insulation Resistance (I.R.) after 60 secs. Charging at rated voltage, 25°C, 55% RH max.		100 GΩ or 1000 MΩ x μF whichever is less	10 GΩ or 100 MΩ x μF whichever is less		
Voltage Proof, 25°C, 1-5 secs.		2.5 x Rated Voltage	2.5 x Rated Voltage		
Capacitance Aging		0	approx. = 1.5% per decade hour		

Dielectric Code	DIA IEC	Z5U 2E6	Y5V 2F4		
Temperature Characteristics	*1	ΔC+22%,-56% maximum over +10°C to +85°C	ΔC+22%,-82% maximum over -30°C to +85°C		
Operating Temperature Range		+10°C to +85°C	-30°C to +85°C		
Measuring Conditions for Capacitance and D.F.	*2	1KHz, 0.5Vrms	1KHz, 10 Vrms		
Dissipation Factor (D.F.) and Tangent of Loss Angle (tan δ)		4.0% 50V 6.0% 25V	rated voltage		
			5.0%	50V	50V
			7.0%	25V	16V
			10.0%	10V	6.3V
Insulation Resistance (I.R.) after 60 secs. Charging at rated voltage, 25°C, 55% RH max.		10 GΩ or 100 MΩ x μF whichever is less	10 GΩ or 100 MΩ x μF whichever is less		
Voltage Proof, 25°C, 1-5 secs.		2.5 x Rated Voltage	2.5 x Rated Voltage		
Capacitance Aging		approx. = 5% per decade hour	approx. = 3% per decade hour		

Surface Mount Capacitors



## Multilayer Ceramic Chip Capacitors Performance Specifications

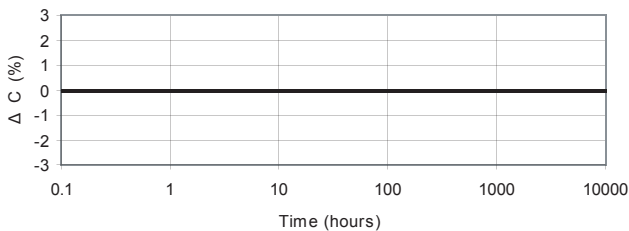
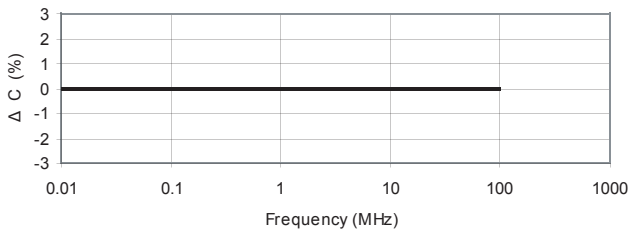
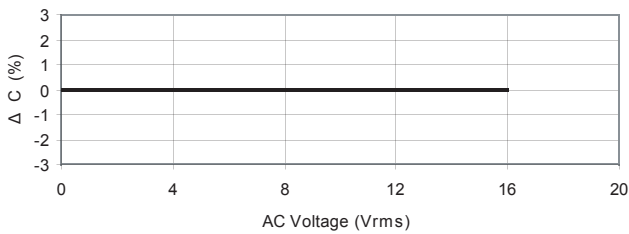
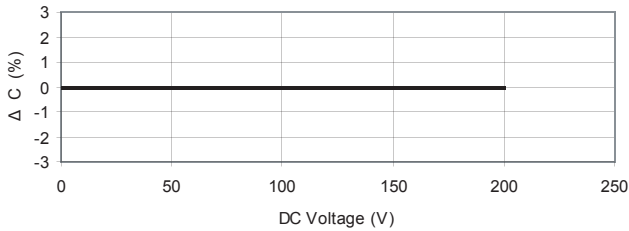
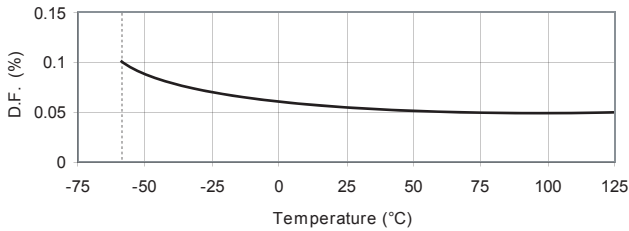
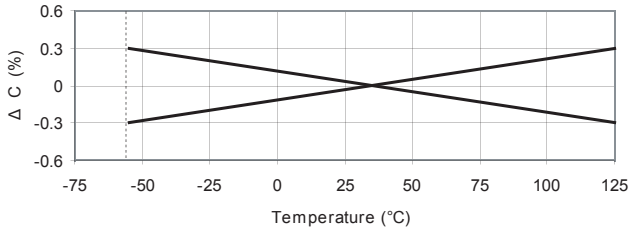
### 2. Environmental

Test	Test Conditions	Post-Test Inspection Requirements					
Solderability	IEC 384-10 4.11/JIS C 5102 8.13 Solder 60 Sn/40 Pb, 235±1 secs. Immersed for 5 secs.	At least 75% of termination area should be well tinned. No visible damage.					
Resistance to Soldering Heat	IEC 384-10 4.10/JIS C 5102 8.14 Immersed in solder bath at 260±5°C for 10±1 secs. Recovery: 6~24 hrs. (COG) 24±2 hrs. (X7R, Z5U, Y5V)	At least 75% of termination area should be covered by solder. No visible damage.					
			<b>COG(1BCG)</b>	<b>X7R(2R1)</b>	<b>Z5U(2E6)</b>	<b>Y5U(2F4)</b>	
		ΔC/C	±0.5%, or ±0.5pF whichever is greater	+ 10%	+20%	+20%	
				-5%	-10%	-10%	
Rapid Change of Temperature	IEC 384-10 4.12/JIS C 5102 9.3 -55°C to + 125°C, 5 cycles(COG,X7R) Duration: 30 mins. Recovery: 6~24 hrs. (COG) 24±2hrs. (X7R)	No visible damage.					
			<b>COG(1BCG)</b>	<b>X7R(2R1)</b>			
		ΔC/C	±1%, or ±1pF whichever is greater			±10%	
		D.F.	1.5 x initial requirement				
		I.R.	0.25 x initial requirement				
Endurance (Life Test)	IEC 384-10 4.15 1000 hrs. at max. temperature with 1.5 x rated voltage applied Recovery: 6~24 hrs. (COG) 24±2 hrs. (X7R, Z5U, Y5V)	No visible damage.					
			<b>COG(1BCG)</b>	<b>X7R(2R1)</b>	<b>Z5U(2E6)</b>	<b>Y5U(2F4)</b>	
		ΔC/C	±2%, or ±1pF whichever is greater	±20%	±20%	±30%	
		D.F.	2.0 x initial req.		1.5 x initial requirement		
		I.R.	0.25 x initial requirement				
Humidity Test (Damp heat, steady state)	IEC 384-10 4.14/JIS C 5102 9.5 500 hrs. at 40±2°C, 90-95% RH Recovery: 6~24 hrs. (COG) 24±2 hrs. (X7R, Z5U, Y5V)	No visible damage.					
			<b>COG(1BCG)</b>	<b>X7R(2R1)</b>	<b>Z5U(2E6)</b>	<b>Y5U(2F4)</b>	
		ΔC/C	±2%, or ±1pF whichever is greater	±10%	±20%	±30%	
		D.F.	2.0 x initial req.		1.5 x initial requirement		
		I.R.	0.25 x initial requirement				
Adhesion	IEC 384-10 4.8/JIS C 5102 8.11.2 Capacitors mounted on a substrate. A force of 5N applied perpendicular to the plane of substrate and parallel the line joining the center of terminations for 10±1 secs.	No visible damage.					

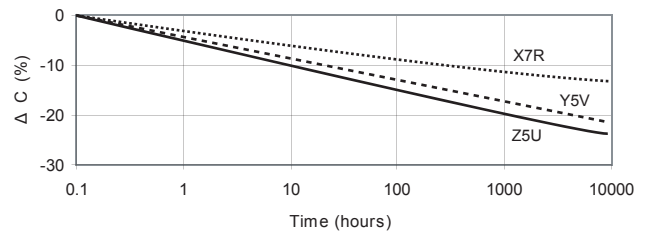
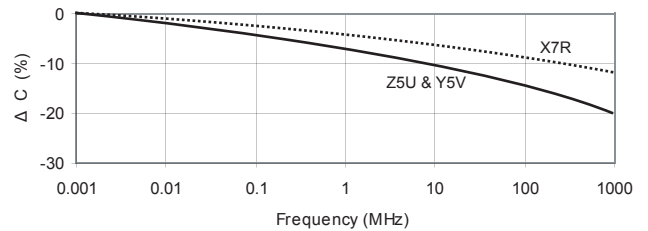
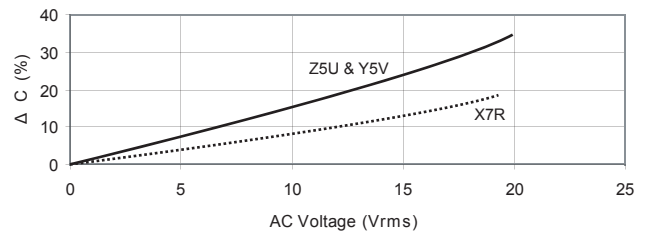
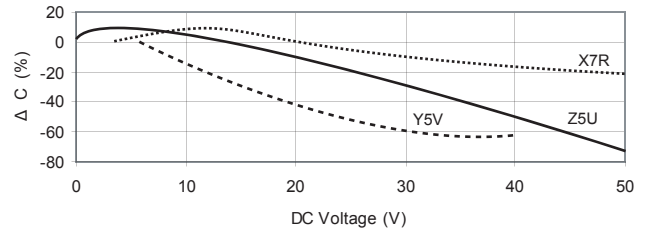
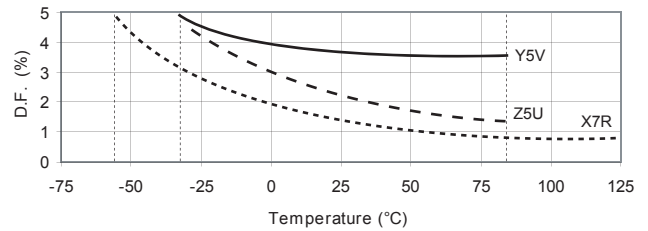
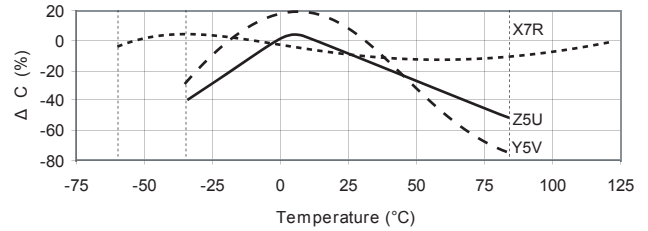
Surface Mount Capacitors



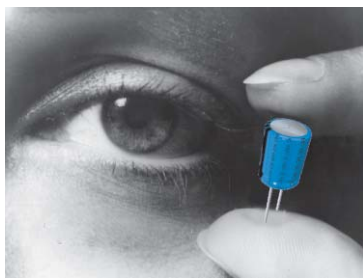
COG(1B)



X7R (2R1), Z5U (2E6), Y5V(2F4)



Surface Mount Capacitors



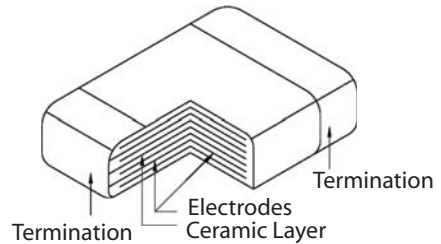
Multilayer Ceramic Chip Capacitors  
Type CMC Series

Δ Features

- Nickel-barrier terminations are finished by electroplated solder
- Nickel barrier layer in terminations prevents dissolution of termination

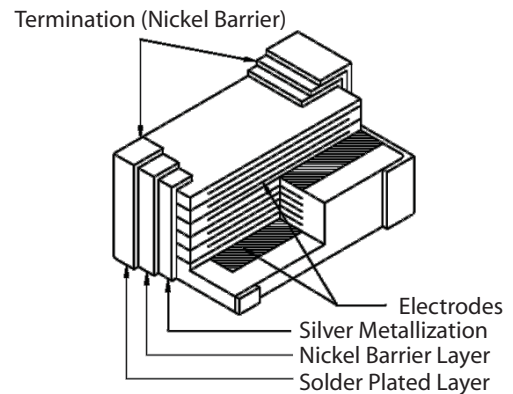
Δ Applications

- Suitable for thick-film hybrid circuits and automatic surface mounting



Δ Resistance to Soldering

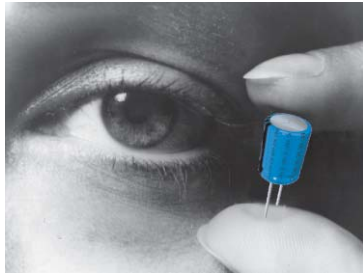
Termination Material	Test Conditions
Nickel-barrier, Solder plated	260 °C, 60 Sn/40 Pb, 10 secs



Δ Tolerances Available

Dielectric		Available Tolerance	Capacitance
EIA	IEC		
COG	1BCG	± 0.25 pF	5 pF
		± 0.5 pF	5pF < CAP < 10 pF
		± 1%, ±2%, ±5%, ±10%	10 pF
X7R	2R1	± 5%, ±10%, ±20%	All values
Z5U	2E6	± 20%, +80% ~ -20%	All values
Y5V	2F4	± 20%, +80% ~ -20%	All values

Surface Mount Capacitors



Multilayer Ceramic Chip Capacitors  
Application Notes

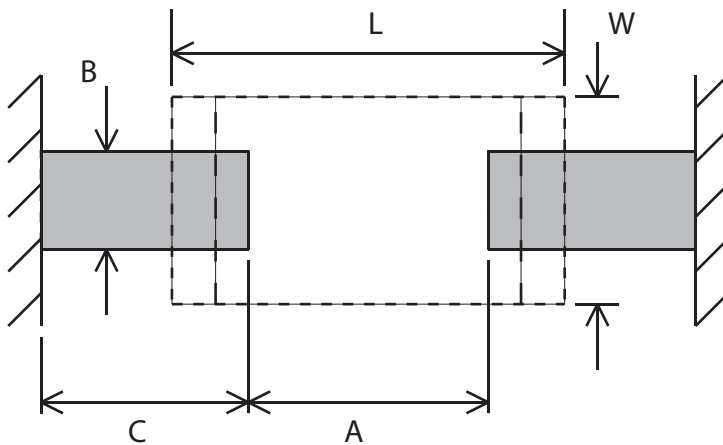
COOLING

After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommend to minimize stress in the colder joint. A cooling rate not exceeding 4° C/sec should be used when forced cooling is necessary.

CLEANING

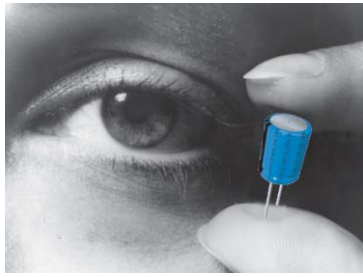
All flux residues must be removed by using suitable electronix-grade vapor-cleaning solvents to eleiminate contamination that could cause electrolytic-surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system is dependent upon many factors such as componenet mix, flux, and solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.

RECOMMENED PAD DIMENSIONS (for reflow soldering)



Unit: mm (inch)

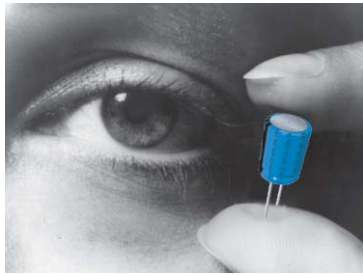
Chip Size	L	W	A	B	C
<b>0603</b>	1.6 (0.063)	0.8 (0.032)	0.6~0.8 (0.024~0.032)	0.6~0.8 (0.024~0.032)	0.6~0.7 (0.024~0.028)
<b>0805</b>	2.0 (0.080)	1.2 (0.050)	1.0~1.2 (0.039~0.047)	0.8~1.1 (0.032~0.043)	0.6~0.7 (0.024~0.028)
<b>1206</b>	3.2 (0.126)	1.6 (0.063)	2.2~2.4 (0.087~0.094)	1.0~1.4 (0.039~0.055)	0.8~0.9 (0.032~0.035)
<b>1210</b>	3.2 (0.126)	2.5 (0.100)	2.0~2.4 (0.080~0.094)	1.8~2.3 (0.071~0.091)	1.0~1.2 (0.039~0.047)
<b>1808</b>	4.5 (0.177)	2.0 (0.080)	2.8~3.4 (0.110~0.134)	1.4~1.8 (0.055~0.071)	1.2~1.4 (0.047~0.055)
<b>1812</b>	4.5 (0.177)	3.2 (0.126)	3.0~3.5 (0.118~0.138)	2.3~3.0 (0.091~0.118)	1.2~1.4 (0.047~0.055)



Multilayer Ceramic Chip Capacitors  
 Type CMC Series  
 Z5U  
 EIA/IEC Dielectric Code: Z5U/2E6

EIA/IEC Dielectric Code	Size		0603		0805		X7R / 2R1		1206		1210		1812	
	(L) Length mm(in)	(W) Width mm(in)	(L) Length mm(in)	(W) Width mm(in)	(L) Length mm(in)	(W) Width mm(in)	(L) Length mm(in)	(W) Width mm(in)	(L) Length mm(in)	(W) Width mm(in)	(L) Length mm(in)	(W) Width mm(in)	(L) Length mm(in)	(W) Width mm(in)
(L) Length mm(in)	1.60±0.15(0.063±0.006)	0.08±0.15(0.032±0.06)	2.00±0.20(0.080±0.008)	1.20±0.20(0.050±0.008)	3.20±0.20(0.126±0.008)	1.60±0.20(0.063±0.008)	3.20±0.20(0.126±0.008)	2.50±0.30(0.100±0.012)	3.20±0.30(0.126±0.012)	4.50±0.30(0.177±0.012)	3.20±0.30(0.126±0.012)	3.20±0.30(0.126±0.012)	4.50±0.30(0.177±0.012)	3.20±0.30(0.126±0.012)
(W) Width mm(in)	0.08±0.15(0.032±0.06)	0.40±0.20(0.16±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.64±0.38(0.025±0.015)	0.64±0.38(0.025±0.015)	0.64±0.38(0.025±0.015)	0.64±0.38(0.025±0.015)	0.64±0.38(0.025±0.015)
(E) Termination mm(in)	0.40±0.20(0.16±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)	0.50±0.20(0.020±0.008)
W.V.D.C.	25	50	25	50	25	50	25	50	25	50	25	50	25	50
Cap. (pF)	2700													
	3300													
	3900													
	4700													
	5600													
	6800													
	8200													
Cap. (µF)	0.01													
	0.012													
	0.015													
	0.018													
	0.022													
	0.027													
	0.033													
	0.039													
	0.047													
	0.056													
	0.068													
	0.082													
	0.1													
	0.12													
	0.15													
	0.18													
	0.22													
	0.27													
	0.33													
	0.39													
	0.47													
	0.56													
	0.68													
	0.82													
	1													
	1.2													
	1.5													
	1.8													

Surface Mount Capacitors



Multilayer Ceramic Chip Capacitors  
 Type CMC - High Voltage Series  
 Z5U  
 EIA/IEC Dielectric Code: Z5U/2E6

EIA/IEC Dielectric Code		Z5U / 2E6				
W.V.D.C.		100V			250V	
Cap. (pF)	Size	0805	1206	1210	1812	1812
.033						
.039						
.047						
.056						
.068						
.082						
.10						
.12						
.15						
.18						
.22						
.27						
.33						
.39						
.47						
.56						
.68						
.82						
1.0						
1.2						
.15						

Surface Mount Capacitors